AMENDMENTS TO THE SPECIFICATION

Please amend paragraphs [01], [02] and [28] of the specification as follows:

[01] This application makes reference to, claims priority to, and claims the benefit of United States Provisional Application Serial No. [[_____]] 60/547,366 ~~(Attorney Docket No. 15574US01)~~ filed February 24, 2004 and entitled "Method and System for Antenna Selection Diversity and Dynamic Gain Control."

[02] This application makes reference to:

United States Utility Application Serial No. [[_____]] 10/810,462 ~~(Attorney Docket No. 15574US02)~~ filed March 26, 2004.

United States Utility Application Serial No. [[_____]] 10/810,433 ~~(Attorney Docket No. 15575US02)~~ filed March 26, 2004.

United States Utility Application Serial No. [[_____]] 10/810,186 ~~(Attorney Docket No. 15624US02)~~ filed March 26, 2004.

[28] FIG. 1A is a diagram of an exemplary receiver system that may be utilized in connection with selection diversity with dynamic gain control, in accordance with an embodiment of the invention. Referring to FIG. 1A, the receiver system 100 may comprise at least one antenna 102, an antenna switch 104, a processor 106,

and a memory 108. There may be as many as M antennas 102 coupled to the antenna switch 104. The antenna 102 may be part of an independent antenna array of antennas coupled to the antenna switch 104, may be one of several individual antennas coupled to the antenna switch 104, and/or may be one of several integrated individual antennas and/or may be part of an integrated array of antennas coupled to the antenna switch 104. The antenna switch 104 may be a mechanical, electronic, electromechanical, and/or microelectromechanical (MEM) switch. The processor ~~102~~ 106 may be a hardware resource, a core processor, a coprocessor, a digital signal processor, or a microcontroller. The memory 108 may be an external memory, an embedded memory, a shared memory, or a main memory. The memory 108 may be an SRAM and/or DRAM type memory.